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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,785	10/29/2003	Makoto Kidera	67162-028	6058

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EXAMINER	
ROSSOSHEK, YELENA	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,785	KIDERA, MAKOTO	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/694,785 filed 10/29/2003.

2. Claims 1-3 are pending in the Application.

Claim Objections

3. Claim 1 is objected to because of the following informalities:

claim 1 line 2 after "of" delete ";" insert --:--

claim 1 line 11 after "plurality of" delete "first"

claim 1 line 11 after transistor" insert –s,--

claim 1 line 19 after "plurality of" delete "first"

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US Patent Publication 2002/0165704).

With respect to claims 1 Yang et al. teaches a method for simulating an electric characteristic of a circuit including transistors within simulation program with SPICE model parameters for an integrated circuit with respect to various electrical

characteristics (abstract) including statistical model parameters for devices containing transistors (paragraph [0006]), comprising the steps of: arranging a plurality of transistors in a matrix pattern on the basis of sizes of the transistors within plurality of NMOS transistors (paragraph [0029]) with consideration of the their sizes (paragraph [0006]), and storing data of the electric characteristic measured on first transistors among the plurality of transistors in the matrix pattern within step 201 of the Fig. 2 for measuring typical data and worst-case data (storing as a model) with respect to various electrical characteristics of the semiconductor devises (transistors) (paragraph [0027]); when a position of a second transistor different from the first transistors is specified in the matrix pattern, determining data of the electric characteristic of the second transistor according to interpolation rules by using the measured data of the one or more first transistors if there are one or more first transistors in the plurality of first transistor at one or more positions adjacent to the position of the second transistor in the matrix pattern within plurality of NMOS transistors having plurality of gates (paragraph [0029]) and extrapolating typical model parameters for each transistor from the plurality of transistors, wherein measured data of electrical characteristics for the previous transistor is used to predict (determine) typical model parameter set as a step 204 of the Fig. 2 using extrapolating preliminary model parameters using the typical data, which was measured for the previous transistor (from the different position in the matrix) (paragraph [0027]); and when a position of a third transistor different from the first and second transistors is specified in the matrix pattern, determining data of the electric characteristic of the third transistor according to the interpolation rules by using the

measured data of the one or more first transistors and/or the interpolated data of the second transistor if there are one or more first transistors in the plurality of first transistor and/or one or more second transistor at one or more positions adjacent to the position of the third transistor in the matrix pattern within plurality of NMOS transistors having plurality of gates (paragraph [0029]) and extrapolating typical model parameters for each transistor from the plurality of transistors, wherein measured data of electrical characteristics for the previous transistor is used to predict (determine) typical model parameter set as a step 204 of the Fig. 2 using extrapolating preliminary model parameters using the typical data, which was measured for the previous transistor (from the different position in the matrix) (paragraph [0027]), wherein SPICE is a program that solves equivalent equations representing the electrical characteristics of a unit device taking into consideration the number of devices used and the electrical connections among the devices (paragraph [0003]). However Yang et al. does not explicitly disclose **interpolation** for determining (predicting) electrical characteristics of the next transistor using measured data of the electrical characteristics of the previously considered transistor (adjacent). Yang et al. substitutes interpolation by extrapolation SPICE mode parameters. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Yang et al. to teach determining a set of typical SPICE model parameters using measured typical data by extrapolating preliminary model parameters and determining a set of worst-case SPICE model parameters using typical data (paragraph [0011]) and adding a set of statistical model parameters in order to realize an accurate worst-case dispersion characteristics (paragraph [0045]).

With respect to claims 2 and 3 Yang et al. teaches:

Claim 2: wherein the sizes of the plurality of transistors include gate length and gate width, the matrix pattern is a two-dimensional pattern of gate length and gate width, and the interpolation rules are defined on the basis of a function of the gate length and the gate width of the transistors as shown on the Figs. 3A and 3B, wherein a graph of threshold voltages of NMOS transistors with respect with dispersion is depicted including relationship between length and width of the gates included into the plurality of transistors and threshold voltages and predicted best-case and worst-case of model parameters (paragraphs [0029], [0030]), wherein best-case and worst-case of model parameters are results of simulating the worst-case SPICE model parameters such as the threshold voltage and saturation current of a device (paragraph [0007]);

Claim 3: wherein the interpolation rules are defined on the basis of a function of gate voltage of the plurality of transistors wherein threshold voltage thereof is taken into account as shown on the Figs. 3A and 3B, wherein a graph of threshold voltages of NMOS transistors with respect with dispersion is depicted including relationship between length and width of the gates included into the plurality of transistors and threshold voltages and predicted best-case and worst-case of model parameters (paragraphs [0029], [0030]), wherein best-case and worst-case of model parameters are results of simulating the worst-case SPICE model parameters such as the threshold voltage and saturation current of a device (paragraph [0007]).

However Yang et al. does not explicitly disclose **interpolation** for determining (predicting) electrical characteristics of the next transistor using measured data of the

electrical characteristics of the previously considered transistor (adjacent). Yang et al. substitutes interpolation by extrapolation SPICE mode parameters. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used Yang et al. to teach determining a set of typical SPICE model parameters using measured typical data by extrapolating preliminary model parameters and determining a set of worst-case SPICE model parameters using typical data (paragraph [0011]) and adding a set of statistical model parameters in order to realize an accurate worst-case dispersion characteristics (paragraph [0045]).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, ~~Matthew S. Smith~~ Jack Chiang can be reached on 571-272-~~1907~~ 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
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